

CLAIMS:

What is claimed is:

1. An apparatus comprising:
  - a processor handling an I/O request in an I/O operation;
  - main storage controlled by the processor for storing data;
  - one or more I/O devices for sending data to or receiving data from said main storage;
  - a vector mechanism operable to register I/O requests by said devices to send or receive data from said main storage;
  - a dispatcher operable to poll said vector mechanism to determine if there is an outstanding I/O request; and
  - an override bit having a first condition when an immediate interrupt is to be sent to said processor for handling an I/O request from said I/O device(s), and a second condition when said dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said override bit being set to its first condition or reset to its second condition by said processor.
2. The apparatus of claim 1 further comprising a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first condition, overrides said TDI value and drives an immediate interrupt to said processor.
3. The apparatus of claim 1 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor for setting the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

1 4. The apparatus of claim 3 further comprising one or more central processing units (CPUs)  
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the  
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 5. The apparatus of claim 1 wherein said override bit is reset to its second condition after an  
2 interrupt is handled by said processor.

1 6. The apparatus of claim 5 wherein said override bit is reset to its second condition after said  
2 dispatcher polls said vector mechanism, said resetting of said override bit to its second condition  
3 upon the first to occur of said interrupt handling or said dispatcher polling.

1 7. An apparatus controlling the transfer of data in a data processing system having a  
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor  
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main  
4 storage, said apparatus comprising:

5 a vector mechanism operable to register I/O requests by said devices to send or receive  
6 data from said main storage;

7 a dispatcher operable to poll said vector mechanism to determine if there is an outstanding  
8 I/O request;

9 an override bit having a first condition when an immediate interrupt is to be sent to said  
10 processor for handling an I/O request from said I/O device(s), and a second condition when said  
11 dispatcher is to poll said vector mechanism to determine if there is an outstanding I/O request, said  
12 override bit being set to its first condition or reset to its second condition by said processor.

1 8. The apparatus of claim 7 further comprising a Target Delay Interval (TDI) register  
2 containing a TDI value for determining when the vector mechanism should not be polled by said  
3 dispatcher and an interrupt given to said processor, and wherein said override bit, when in its first  
4 condition, overrides said TDI value and drives an immediate interrupt to said processor.

1 9. The apparatus of claim 7 wherein said main storage is divided into multiple partitions, with  
2 each partition having a vector mechanism operable to register I/O requests by said devices to send  
3 or receive data from that partition of main storage, each partition having an associated override bit  
4 for that partition, and said processor is a hypervisor for setting the override bit for that partition  
5 when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for  
6 that partition.

1 10. The apparatus of claim 9 further comprising one or more central processing units (CPUs)  
2 assignable by said hypervisor to one or more of said partitions, said hypervisor further setting the  
3 override bit of one partition when that partition does not have a CPU assigned to it.

1 11. The apparatus of claim 7 wherein said override bit is reset to its second condition after an  
2 interrupt is handled by said processor.

1 12. The apparatus of claim 11 wherein said override bit is reset to its second condition after  
2 said dispatcher polls said vector mechanism, said resetting of said override bit to its second  
3 condition upon the first to occur of said interrupt handling or said dispatcher polling.

1 13. A method for controlling the transfer of data in a data processing system having a  
2 processor handling an I/O request in an I/O operation, main storage controlled by the processor  
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main  
4 storage, said method comprising:

5 registering in a vector mechanism, I/O requests by said devices to send or receive data  
6 from said main storage;

7 polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O  
8 request; and

9 sending an immediate interrupt to said processor when an override bit has a first condition  
10 for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector  
11 mechanism to determine if there is an outstanding I/O request when said override bit is in a second  
12 condition.

1 14. The method of claim 13 wherein said data processing further includes a Target Delay  
2 Interval (TDI) register containing a TDI value for determining when the vector mechanism should  
3 not be polled by said dispatcher and an interrupt given to said processor, said method further  
4 comprising overriding said TDI value and driving an immediate interrupt to said processor when  
5 said override bit is in its first condition.

1 15. The method of claim 13 wherein said main storage is divided into multiple partitions, with  
2 each partition having a vector mechanism operable to register I/O requests by said devices to send  
3 or receive data from that partition of main storage, each partition having an associated override bit  
4 for that partition, and said processor is a hypervisor, said method further comprising setting by said  
5 hypervisor the override bit for that partition when said hypervisor is to handle an immediate  
6 interrupt rather than polling by said dispatcher for that partition.

1 16. The method of claim 15 wherein said data processing system further includes one or more  
2 central processing units (CPUs) assignable by said hypervisor to one or more of said partitions,  
3 said method further comprising setting by said hypervisor, the override bit of one partition when  
4 that partition does not have a CPU assigned to it.

1 17. The method of claim 13 further comprising resetting said override bit to its second  
2 condition after an interrupt is handled by said processor.

1 18. The method of claim 17 further comprising resetting said override bit to its second  
2 condition upon the first to occur for said interrupt handling or said dispatcher polling.

1 19. A program product for controlling the transfer of data in a data processing system having  
2 a processor handling an I/O request in an I/O operation, main storage controlled by the processor  
3 for storing data, and one or more I/O devices for sending data to or receiving data from said main  
4 storage, said program product comprising:

5 a computer readable medium having recorded thereon computer readable program code  
6 means for performing the method comprising:

7           registering in a vector mechanism, I/O requests by said devices to send or receive data  
8   from said main storage;  
9           polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O  
10   request; and  
11           sending an immediate interrupt to said processor when an override bit has a first condition  
12   for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector  
13   mechanism to determine if there is an outstanding I/O request when said override bit is in a second  
14   condition..

1   20.    The program product of claim 19 wherein said data processing further includes a Target  
2   Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism  
3   should not be polled by said dispatcher and an interrupt given to said processor, said method  
4   further comprising overriding said TDI value and driving an immediate interrupt to said processor  
5   when said override bit is in its first condition.

1   21.    The program product of claim 19 wherein said main storage is divided into multiple  
2   partitions, with each partition having a vector mechanism operable to register I/O requests by said  
3   devices to send or receive data from that partition of main storage, each partition having an  
4   associated override bit for that partition, and said processor is a hypervisor, said method further  
5   comprising setting by said hypervisor the override bit for that partition when said hypervisor is to  
6   handle an immediate interrupt rather than polling by said dispatcher for that partition.

1   22.    The program product of claim 21 wherein said data processing system further includes one  
2   or more central processing units (CPUs) assignable by said hypervisor to one or more of said  
3   partitions, said method further comprising setting by said hypervisor, the override bit of one  
4   partition when that partition does not have a CPU assigned to it.

1   23.    The program product of claim 19 wherein said method further comprises resetting said  
2   override bit to its second condition after an interrupt is handled by said processor.

Year	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	